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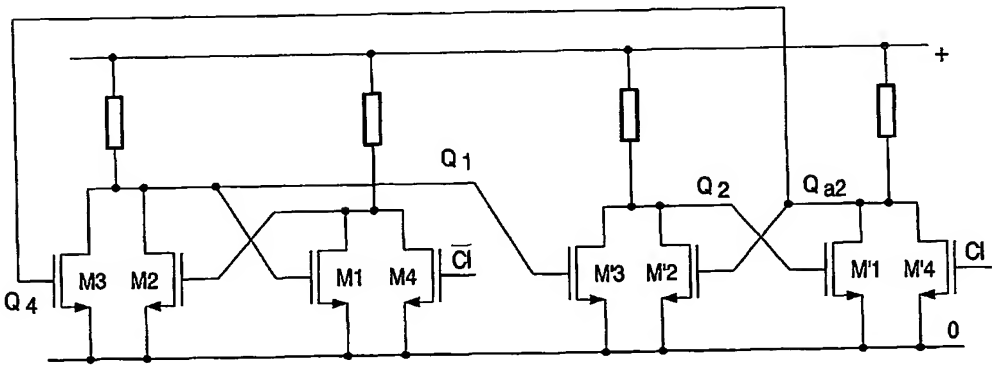
(54) Title: FREQUENCY DIVIDER



(57) Abstract: A frequency divider comprising a first flip-flop (M1, M2, M3, M4) having a first clock input (CI) for receiving a clock signal, the flip-flop further comprising a first set input (Q4) and a first non-inverted output (Q1). The frequency divider further comprises a second flip-flop (M'1, M'2, M'3, M'4) having a second clock input (CI) for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input (CI), a second set input coupled to the first non-inverted output (Q1), a second non-inverted output (Q2) and a second inverted output (Q2), the second inverted output (Q2) being coupled to the first set input (Q4).

WO 2005/041413 A1

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